

CLAIMS

What is claimed is:

1. A method for driving a data signal across a data bus, comprising:

charging the data bus to a first voltage level;

5 maintaining the data bus at the first voltage level when a first type of data signal is to be driven across the data bus; and

pulling the data bus to a second voltage level when a second type of data signal is to be driven across the data bus.

10 2. The method of claim 1, wherein: the first type of data signal is a high data signal; and the second type of data signal is a low data signal.

3. The method of claim 1, wherein the first voltage level is about 1.8 Volts.

15 4. The method of claim 1, wherein the first level voltage level corresponds to a power supply voltage level.

5. The method of claim 1, wherein the first type of data signal corresponds to the binary digit “1”.

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6. The method of claim 1, wherein maintaining the data bus at the first level comprises connecting the data bus to a power supply voltage source.

7. The method of claim 1, wherein maintaining the data bus at the first level comprises connecting the data bus to ground.

8. The method of claim 1, wherein the second voltage level is about 0.0 Volts.

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9. The method of claim 1, wherein the second type of data signal corresponds to the binary digit “0”.

10. The method of claim 1, wherein pulling the data bus to the second voltage level comprises connecting the data bus to a power supply voltage source.

11. The method of claim 1, wherein pulling the data bus to the second voltage level comprises connecting the data bus to ground.

15 12. The method of claim 1, wherein the step of pulling the data bus to a second voltage level comprises turning on a transistor so that current flows through the transistor from the data bus to ground.

20 13. The method of claim 1, wherein the step of pulling the data bus to a second voltage level comprises turning on a transistor so that current flows through the transistor from a power supply voltage source to the data bus.

14. A system for driving a data signal, comprising:
a data bus;

a charging circuit coupled to the data bus, wherein the charging circuit is configured to charge the data bus to a first voltage level; and

a pull-down circuit coupled to the data bus, wherein the pull-down circuit is configured to pull the data bus to a second voltage level.

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15. The system of claim 14, further comprising a keeper circuit coupled to the data bus, wherein the keeper circuit is configured to maintain the data bus at the first voltage level after the data bus has been charged.

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16. The system of claim 14, wherein the pull-down circuit comprises:
a transistor coupled at one end to the data bus and at the other end to ground;
logic circuitry coupled to a gate of the transistor, wherein an output signal from the logic circuitry controls the transistor.

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17. The system of claim 16 wherein the logic circuitry comprises a first input terminal for receiving an equilibration signal and a second input terminal for receiving a data signal.

18. The system of claim 14, wherein the logic circuitry comprises a NOR gate.

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19. The system of claim 14, wherein the charging circuit comprises:
a transistor coupled at one end to a power supply voltage source and at the other end to the data bus, wherein the transistor is controlled by an equilibration signal.

20. The system of claim 15, wherein the keeper circuit comprises:

a transistor coupled at one end to a power supply voltage source and at the other

end to the data bus; and

logic circuitry coupled to a gate of the transistor, wherein an output signal from the

5 logic circuitry controls the transistor.

21. The system of claim 20, wherein the logic circuitry comprises an inverter

gate.